# FRAMEWORK WITH MULTIPLE SELECTIONS FOR SOUTH BRIDGE AND NORTH BRIDGE CONNECTING

## CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of U.S.A provisional application serial no. 60/225,018, filed August 11, 2000, and Taiwan application serial no. 90117039, filed July 12, 2001.

## BACKGROUND OF THE INVENTION

Field of the Invention

**[0001]** The invention relates in general to a framework with multiple selections to connect between a north bridge and a south bridge, and more particularly, to a variety of connection controls applied between south and north bridges.

Description of the Related Art

**[0002]** Most of the chip sets to control all the devices on the current computer boards normally comprise a north bridge and a south bridge. The north bridge is used to manage the data transmission between the central processing unit (CPU), the master memory and the accelerated graphics port (AGP). The data transmission for the I/O ports (parallel/serial ports), USB, keyboard controller, AC97 audio card, floppy disk controller and IDE controller are all covered under the south bridge. The north and south bridges communicate via a PCI bus. Referring to Figure 1A, a block diagram for a conventional connection structure between the south and north bridges is shown. The north bridge 10

is respectively connected to the CPU 12, the dynamic random access memory (DRAM) 14, the 3D graphics controller 16 and the PCI bus 32. The south bridge 20 is connected to a plurality of PCI slots via a PCI bus 32. The above is the common computer motherboard structure used currently. When the south bridge 20 communicates with the PCI bus 32, a request signal REQ is provided by the PCI master controller 202. After the request signal REQ is granted (GNT), a message communication is allowed between the direct memory access engine 200 and the PCI bus 32. When the north bridge 10 communicates with the PCI bus 32, the message is transmitted from the memory controller 100 through the PCI response 102 and the PCI bus 32. Conversely, when the PCI slot 30 has to communicate with the north bridge 10, a request signal REQ is output. Being granted by the arbiter 104, the information can be transmitted from the PCI bus 32 to the north bridge 10. As a PCI bus 32 and a multiplicity of PCI slots 30 are required to complete the communication between the north bridge 10 and the south bridge 20, the speed of the north chip 10 is slow. Further, many pins of the north bridge 10 are occupied by the PCI bus 32 to limit the development of such a structure.

**[0003]** To overcome the limited bandwidth of the conventional north and south bridges, a high speed CPU and a double data rate (DDR) memory can be used. Due to the restriction of the transmission function and insufficient functionalities, the high speed function of the DDR motherboard cannot be achieved. Therefore, a technique of a private link bus to connect the north and south bridge has been developed. The bandwidth of the north and south bridges is increased to 266MB, which doubles the conventional communication speed of the north and south bridges. Applying the characteristics of high efficiency and high bandwidth, the quality of I/O data transmission is very much

enhanced, especially for audio-video transmission. Referring to Figure 1B, a conventional structure using a private link bus to communicate between the south and north bridges is shown. A north bridge 10' is provided and connected to the CPU 12, the DRAM 14 and the 3D graphics bus 16. A memory controller 100' uses a high speed bus 20V to connect the south bridge 20'. The south bridge 20' is further connected to the PCI bus 32, via which a plurality of PCI slots 30 is connected. In the south bridge 20', an arbiter 206', a PCI response 204' and an up/down controller 201' are further provided. The direct memory access engine 200' can thus select path 201'a to the high speed bus 20V via the up/down controller 201', or the path 201'b to the PCI master controller 202'. This kind of structure is applied to a higher standard computer. Since the north bridge 10' and the south bridge 20' respectively have their own bus, the speed is much faster. The pins of the south bridges 10' are free from the connection of the PCI bus 32, and a future expandability is allowed.

**[0004]** However, in the above two structures, the south and north bridges are not compatible with each other. Four kinds of control chips are required for their manufacture. While a new product is designed, a lot of labor and cost are required since these two structures have to be modified separately. This further causes a burden in inventory, and thus, increases the manufacturing cost.

## SUMMARY OF THE INVENTION

**[0005]** The invention provides a connection apparatus and method with multiple selections between the north and south bridges. The connection structure can be operated under different modes according to the peripheral and chip circuit design. A great deal of

labor and material cost is saved. Further, the risk of controlling and storing four control chips is eliminated.

**[0006]** The framework with multiple selections to connect the south and north bridges comprises a south bridge and a north bridge. The north bridge has a memory controller, a PCI response, and a master bus arbiter. The memory controller is coupled to a random access memory to control the memory access. The PCI response (PCI-S) is connected between the memory controller and the PCI bus for data response process. The master bus arbiter connected to the PCI response is provided with a plurality of request signal terminals and a plurality of grant signal terminals respectively connected to apparatus on the PCI bus to arbitrate whether the data transmission of such apparatus is granted.

**[0007]** The south bridge includes a high speed bus interface, which further has a direct memory access engine (DMA engine), an up/down controller, a PCI master controller, and a sub-bus arbiter. The direct memory access engine has an output terminal to output a direct memory access request signal. The up/down controller is connected to the output terminal of the direct memory access engine to receive the direct memory access request signal, to control the data transmission direction. The up/down controller has a plurality of output terminals. The PCI master controller (PCI-M) is connected to the PCI bus and one output terminal of the up/down controller. When the output terminal is outputting the direct memory access request signal, it automatically sends a data access transaction to the PCI bus. The sub-bus arbiter is connected to the PCI master controller and has a plurality of request signal terminals and a plurality of grant signal terminals respectively connected to the master bus arbiter of the north bridge.

**[0008]** Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** Figure 1A shows a block diagram of a conventional connection structure between north and south bridges;

**[0010]** Figure 1B shows a block diagram using a private link bus interface to north and south bridges; and

**[0011]** Figures 2 shows a block diagram of a framework to connect north and south bridges according to the invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0012]** In Figure 2, a block diagram of a framework to connect the south and north bridge is shown. The structure of Figure 2 uses the concept of inversing the south bridge 20' illustrated in Figure 1B. The south bridge 50 and north bridge 40 are both operated on the PCI bus 62, so that the request signal of the direct memory access engine 500 of the south bridge 50 can only be output from the PCI bus 62. The output terminal 501a of the up/down controller 501 is therefore disabled. As a result, the signal of the output terminal of the direct memory access engine 500 has to be transmitted from another output terminal 501b of the up/down controller 501 through the PCI master controller 502 first, then to the PCI bus 62. The north bridge and other PCI compatible devices are all connected to the PCI bus 62, therefore the DMA request signal can be sent to the PCI bus

and each apparatus can then extract the DMA request signal from the PCI bus 62. The PCI response 504 is also disabled, so that a response to the PCI bus 62 is sent by the PCI response 402 of the north bridge 40 to avoid the PCI responses 402 and 504 fighting for data. The bus arbiter of the PCI bus 62 is dominated by the main bus arbiter 404 of the north bridge 40 as the master bus arbiter. When the south bridge 50 requests using the PCI bus 62, the sub-bus arbiter 506 sends a first request signal and receives a first grant signal to determine whether the right of using the PCI bus 62 is obtained. It is known to people of ordinary skill in the art that the request signal can be output from the grant signal terminal 54, while the grant signal can be received by the request signal terminal 56. When the master bus arbiter and the sub-bus arbiter are serially connected, the sub-bus arbiter 506 sends the first request signal via one of the request signal terminals 56, and receives a first grant signal via one of the grant signal terminals 54. When the master bus arbiter has to connect many PCI compatible apparatuses and there are not enough pins, the sub-bus arbiter 506 can be connected to the master bus arbiter 404 in series, so as to provide additional pins for the PCI compatible apparatuses. The PCI compatible apparatuses then send request signals to the master bus arbiter 404 via the sub-bus arbiter 506, and receive grant signals from the master bus arbiter 404 via the sub-bus arbiter 506.

**[0013]** According to the invention, a framework with multiple selections to connect between south and north bridges is provided. The manufacturers fabricating PCI bus chips and motherboards do not have to control two kinds of bus control chips. Instead, only one PCI bus control chip is required that operates under two modes. The labor and cost consumption is greatly saved, and the risk of large inventory is eliminated.

**[0014]** Other embodiments of the invention will appear to those skilled in the art

from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples are to be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.